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PATENT APPLICATION AF

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Debendra Das Sharma

Confirmation No.:

Application No.: 10/011,857

Examiner: Khang Dang

Filing Date: NOV. 5, 2001

Group Art Unit:

Title: METHOD AND SYSTEM FOR CONTROLLING FLOW OF ORDERED, PIPELINED TRANSACTIONS BETWEEN INTERCOMMUNICATING ELECTRONIC DEVICES

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF REPLY BRIEF

Sir:

Transmitted herewith in ***triplicate*** is the Reply Brief with respect to the Examiner's Answer mailed on **March 24, 2006**. This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new grounds of rejection.)

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Respectfully submitted,

Debendra Das Sharma

By Robert W. Bergstrom

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Date: **May 24, 2006**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant:	Debendra Das Sharma
Application No.:	10/011,857
Filed:	November 5, 2001
Title:	Method and System for Controlling Flow of Ordered, Pipelined Transactions between Intercommunicating Electronic Devices
Examiner:	Khanh Dang
Art Unit:	2111
Docket No.:	10017812-1
Date:	May 24, 2006

REPLY BRIEF UNDER 37 CFR 1.193(b)(1)

Mail Stop Board of Patent Appeals and interferences
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Examiner's Answer dated March 24, 2006, Appellant replies as follows:

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

Appellant's Representative has not identified, and does not know of, any other appeals of interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF AMENDMENTS

No Amendment After Final is enclosed with this brief. The last Amendment was filed August 4, 2004. Appellant's amendments in an Amendment After Final filed on September 21, 2005, were not considered and were not entered into the record by the Examiner.

SUMMARY OF CLAIMED SUBJECT MATTER

Overview

One embodiment of the present invention is directed to a method and system for guaranteeing in-order delivery of transaction requests (1010-1018 in Figure 10A) from a producing node, such as a bus bridge (106-107 in Figure 1) or other processing entity or other computer-system component, and a consuming node, such as a bus bridge (108 in Figure 1) or other processing entity or other computer-system component. In the producing node, outstanding transaction requests are maintained within a source input queue (1002 in Figure 10A), each transaction request associated with a retry bit. When a message is transmitted from the producing node to the consuming node, a special marker bit (1040 in Figure 10E) may be included to flag certain messages as special to the consuming node. The consuming node maintains a retry vector (1006 in Figure 10A) having a retry bit corresponding to each producing node. When the producing node receives a NAK reply (1036 in Figure 10C) from the consuming node rejecting a transaction request, the producing node sets the retry bit for the transaction request in the source input queue, as well as the retry bits for other pending, subsequently received transaction requests directed to the consuming node. The producing node then proceeds to retransmit the transaction request and any additional pending, subsequently received transaction requests to the consuming node. When the producing node transmits the oldest transaction request (1038 in Figure 10E) pending for a particular consuming node, the producing node sets the special marker bit within the transaction request

to flag the transaction request to the consuming node. When a consuming node receives a transaction request from the producing node, it first checks the retry vector to determine whether or not the retry vector bit corresponding to the producing node has been set. If so, then the consuming node responds with a NAK reply unless the special marker bit within the transaction request is set. If the special marker bit is set, and if the retransmitted transaction request can now be accommodated by the consuming node, the consuming node resets the bit within the retry vector corresponding to the producing node and replies with an ACK reply to the producing node. This technique guarantees that, once the consuming node rejects a transaction request within an ordered stream of transaction requests, the transaction request will be retransmitted by the producing node within a proper ordering of transaction requests.

Independent Claim 1

Claim 1 claims a method for controlling flow of requests and replies between a first electronic device, such as such as a bus bridge (106-107 in Figure 1), that stores new and pending requests in an electronic memory and retrieves new and pending requests from the electronic memory for transmission, as in a source input queue (1002 in Figure 10A), and a second electronic device, such as such as a bus bridge (106-107 in Figure 1), that accepts requests transmitted from the first electronic device, transmitting back to the first electronic device an ACK reply (1028 in Figure 10B), and rejects requests transmitted from the first electronic device, transmitting back to the first electronic device a NAK reply (1036 in Figure 10C). The method of claim 1 includes steps of: (1) storing by the first electronic device a retry bit associated with each stored request (*see* retry bits in entries in the source input queue, 1002 in Figures 10A-H); (2) storing by the second electronic device a retry vector (1006 in Figure 10A) containing bits corresponding to a first set of electronic devices from which the second electronic device receives requests; (3) maintaining a copy in storage, such as in source input queue (1002 in Figure 10A), by the first electronic device, of each request until an ACK reply corresponding to the request is received by the second electronic device; (4) employing the retry bits associated with each stored request by the first electronic device to mark requests for retransmission (*see* retry bits set to "1" in Figure 10D) ; and (5) employing the retry vector by the second electronic device to mark a second set of electronic devices that need to retransmit one or more rejected requests (see retry bit marked "1" in retry vector 1006 Figure 10D).

Dependent Claims 2 – 14

Claim 2 is directed to actions taken by the first electronic device upon receiving a NAK reply from the second electronic device. Claim 3 is directed to actions taken by the second electronic device upon receiving a request from the first electronic device: Claim 4 is directed to storing, by the first electronic device, new and pending requests in a source input queue. Claim 5 is directed to a system in which the first electronic device is a source node and the second electronic device is a destination node. Claim 6 is directed to a method practiced in a system in which the first electronic device is a producing node and the second electronic device is a destination node. Claim 7 is directed to a method practiced in a computer system in which the first electronic device is a producing node and the second electronic device is a consuming node. Claim 8 is directed to a method practiced in a computer system in which the first electronic device is a source node and the second electronic device is a consuming node. Claim 9 is directed to a method practiced in a computer system in which the first electronic device is directly connected to the second electronic device by an electronic communications medium. Claim 10 is directed to a method practiced in a computer system in which the first electronic device is indirectly connected to the second electronic device by a first electronic communications medium, a forwarding node, and a second electronic communications medium, the first electronic communications connected to the first electronic device and the forwarding node, and the second electronic communications medium connected to the forwarding node and the second electronic device. Claim 11 is directed to a method practiced in a computer system in which the first electronic device is indirectly connected to the second electronic device by a number of electronic communications media and forwarding nodes. Claim 12 is directed to a method practiced in a computer system in which the first electronic device and second electronic device are bus interconnect components within a computer system. Claim 13 is directed to a method practiced in a system in which each bit of the retry vector corresponds to an electronic device, directly connected to the second electronic device, which can send requests to the second electronic device. Claim 14 is directed to a method practiced in a system in which each bit of the retry vector corresponds to a unique set of electronic devices that originate and forward requests to the second electronic device.

Independent Claim 15

Claim 15 is directed to a system containing two intercommunicating electronic devices, such as a bus bridges (106-107 in Figure 1), comprising: (1) a first electronic device that stores new and pending requests in an electronic memory and retrieves new and pending requests from the electronic memory for transmission, such as source input queue (1002 in Figure 10A); (2) a retry bit associated with each stored request within the first electronic device (*see* retry bits in entries in the source input queue, 1002 in Figures 10A-H); (3) a second electronic device that accepts requests transmitted from the first electronic device, transmitting back to the first electronic device an ACK reply, and rejects requests transmitted from the first electronic device, transmitting back to the first electronic device a NAK reply; and (4) a retry vector (1006 in Figure 10A) maintained by the second electronic device containing retry vector bits corresponding to a set of electronic devices from which the second electronic device receives requests that need to retransmit one or more rejected requests.

Dependent Claims 16 – 20

Claim 16 is directed to a system that, when a request corresponding to a NAK reply is the oldest pending request directed to the second electronic device, sets the retry bits associated with all subsequent requests directed to the second electronic device. Claim 17 is directed to a system that, when a request corresponding to the NAK reply is not the oldest pending request directed to the second electronic device, retransmits the request to the second electronic device without a special marker bit. Claim 18 is directed to a system in which control logic within the second electronic device that receives a request from the first electronic device and, when the retry vector bit corresponding to the first electronic device is set and when no special marker bit is set in the request, sends a NAK reply back to the first electronic device. Claim 19 is directed to a system that, when the retry vector bit corresponding to the first electronic device is not set or a special marker bit is set in a received request, the control logic determines if the request can be processed by the second electronic device and when the request can be processed by the second electronic device, resets the retry vector bit corresponding to the first electronic device and sends an ACK reply

back to the first electronic device. Claim 20 is directed to a system that, when the request cannot be processed by the second electronic device, sets the retry vector bit corresponding to the first electronic device and sends a NAK reply back to the first electronic device.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1 and 4-15 are anticipated by Uchara et al., U2002/0040414 A1 ("Uchara") under 35 U.S.C. § 102(e).

2. Whether claims 1-20 are indefinite under 35 USC § 112, second paragraph.

ARGUMENT

Claims 1-20 are currently pending in the application. In an Office Action dated July 21, 2005 ("Final Office Action"), the Examiner rejected claims 1-20 under 35 USC § 112, second paragraph, as being indefinite, rejected claims 1 and 4-15 under 35 U.S.C. § 102(e) as being anticipated by Uchara et al., U2002/0040414 A1 ("Uchara"), and conditionally allowed claims 2, 3, and 16-20. Appellant filed an Appeal Brief on January 23, 2006 in which Appellant respectfully traverses the 35 USC § 112, second paragraph rejection of claims 1-20 and the 35 U.S.C. § 102(e) rejections of claims 1 and 4-15. The Examiner issued an Examiner's Answer to the Appeal Brief on March 24th, 2006, in which the Examiner apparently included new grounds of rejection with respect to Issue 1, identified above, and maintained the 35 USC § 112, second paragraph rejections in the Office Action. Appellant respectfully traverses the new grounds of rejection with respect to Issue 1 and the Examiner's continued rejections of claims 1-20 under 35 USC § 112, second paragraph.

ISSUE 1

1. Whether claims 1 and 4-15 are anticipated by Uchara under 35 U.S.C. § 102(e).

In an Office Action dated May 4, 2004, the Examiner rejected claims 1 and 4-15 under 35 U.S.C. § 102(e) as being anticipated by Uchara. In a Response filed August 4, 2004, Appellant's representative submitted a 37 CFR § 1.131 Declaration in which Appellant declared that he had conceived of the claimed invention prior to the July 3, 2001 effective date of the cited reference. In the Final Office Action, dated July 21, 2005, the Examiner

stated:

> In response to Applicants' argument, the declaration under 36 CFR 1.131 filed 8/10/2004 is insufficient to overcome the rejection of claims 1, 4-15 over Uchara under 35 USC § 102(e) as set forth in the last Office action because it is not properly executed and fails to establish reduction to practice prior to the date of the reference. ... In the affidavit Applicants state that the invention was reduced to practice. However, a written description does not constitute an actual reduction to practice. Furthermore, only the filing of a US patent application which complies with the disclosure requirement of 35 U.S.C. § 112 constitutes a constructive reduction to practice. A written description, no matter how complete, which has not been made the subject of a US patent application does not qualify as reduction to practice. In any event, it is Applicants' acknowledgement that the invention is not built or tested ...

The Examiner did not indicate why the previously submitted Rule 131 Declaration is not properly executed. It is complete, and is signed and dated by Appellant. The Rule 131 Declaration is directed to the conception of the invention by Appellant prior to the date of the cited reference and diligence in pursuing a constructive reduction to practice. Filing of the Current Application constitutes a constructive reduction to practice. As stated in 37 C.F.R. § 1.131(b):

> The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or conception of the invention prior to the effective data of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application.

In a Response After Final, filed September 21, 2005, Appellant's representative endeavored to assist the Examiner in properly considering the previously filed Rule 131 Declaration. In the Response After Final, Appellant's representative pointed out to the Examiner that the previously filed Rule 131 Declaration establishes conception of the invention prior to the effective date of the reference coupled with due diligence from the prior said date, and, in addition, submitted a newly executed Rule 131 Declaration intended to correct any deficiencies in the originally submitted Rule 131 Declaration, even though the deficiencies were not pointed out clearly by the Examiner, and Appellant's representative did not understand why the previously submitted Rule 131 Declaration was improperly executed. In an Advisory Action dated October 11, 2005, the Examiner apparently maintained the rejections of claims 1 and 4-15, and did not address Appellant's representative's arguments concerning the original Declaration and the second Declaration or explain the Examiner's

position.

Finally, in the Examiner's Answer, issued on March 24, 2006, the Examiner recognizes that the submitted Rule 131 affidavit is intended to show "conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application." The Examiner then lists various criteria used to establish conception, and then concludes that the evidence provided with the originally filed Rule 131 affidavit is insufficient to support Appellant's assertion of prior conception and due diligence. Appellant disagrees.

First, the Examiner, on page 8 of the Examiner's Answer, states that, under MPEP §715.07, "[d]isclosure documents (MPEP §1706) may be used as documentary evidence of conception." The Examiner then states that "[n]one is provided by the Appellants." This statement is incorrect. In the originally submitted Rule 131 affidavit, Appellant stated that Appellant provides an Invention Disclosure. Exhibit 1 included with the Rule 131 Declaration is, in fact, the invention disclosure form prepared by Appellant and submitted to the Hewlett-Packard Corporation Legal Department, and is the Invention Disclosure used by Appellant's representative to prepare the current patent application.

Next, on pages 9-10 of the Examiner's Answer, the Examiner states that the exhibit included in the Rule 131 Declaration, which, in fact, is the Invention Disclosure furnished by Appellant to the Hewlett-Packard Corporation Legal Department and used by Appellant's representative to prepare the current application, does not support all claimed limitations. The Examiner then quotes all but the first part of the preamble of claim 1, apparently intending to indicate that the bulk of claim 1 is not supported by the Invention Disclosure.

Appellant's representative observes that, in general, inventors tend to rather concisely describe their inventions in invention disclosures. They typically do not, for example, provide extensive backgrounds regarding material that would be well known to those familiar with the particular scientific and/or technical fields to which the invention pertains. Appellant's representative also observes that, in general, particular phrasing and terminology used in claims is typically not included in invention disclosures, but arises during drafting of the specification of a patent application. Conception of an invention relates to the idea or essence of an invention, rather than to a particular description of the invention. The essence of the currently claimed invention is most decidedly described in the Invention Disclosure included with the Rule 131 Declaration.

Please consider claim 1, provided below:

> 1. A method for controlling flow of requests and replies between a first electronic device that stores new and pending requests in an electronic memory and retrieves new and pending requests from the electronic memory for transmission, and a second electronic device that accepts requests transmitted from the first electronic device, transmitting back to the first electronic device an ACK reply, and rejects requests transmitted from the first electronic device, transmitting back to the first electronic device a NAK reply, the method comprising:
>
> storing by the first electronic device a retry bit associated with each stored request;
>
> storing by the second electronic device a retry vector containing bits corresponding to electronic devices from which the second electronic device receives requests;
>
> maintaining a copy in storage, by the first electronic device, of each request until an ACK reply corresponding to the request is received by the second electronic device;
>
> employing the retry bits associated with each stored request by the first electronic device to mark requests for retransmission; and
>
> employing the retry vector by the second electronic device to mark electronic devices that need to retransmit one or more rejected requests.

The preamble of claim 1 describes a general transaction model typically employed in intercommunicating electronic devices. In the first sentence of Part A on the third page of the Invention Disclosure, Appellant states:

> Sometimes enforcing ordering between transactions in a computer system becomes necessary. A good example of this is PIO transactions. PIO writes coming from a processor should not get out of order for the programming model to work. Processors normally pipeline PIO Writes (issue subsequent PIO Writes without getting the commit for the earlier PIOs) for improved performance. It is left up to the chips in the interconnection network to guarantee that they be delivered in order. Another requirement is the capability to retry (or nack) the transaction if there is not enough resources to serve the transaction request instead of blocking the queue and letting other transactions suffer.

Appellant assumes the reader to be familiar with programmed input/output ("PIO"). The ordinarily skilled reader knows that PIO is an interface originally developed for transfer of data between processors and ATA disk controllers, and that the term is applied more generally in various systems of intercommunicating hardware devices. The above-quoted portion of the Invention Disclosure discusses transactions, retry of transactions based on a nack, also referred to as "NAK" in computer science and communications, and refers to a

transaction queue described by the preamble language: "stores new and pending requests in an electronic memory and retrieves new and pending requests from the electronic memory for transmission." Appellant obviously presumed the reader to be familiar with general transaction models, ACK and NAK responses to requests, and other such familiar computational and communications notions. Protocols that employ NAK responses generally also employ ACK responses.

In Part C on the third page of the Invention Disclosure, Appellant outlines the invention described in the current application and claimed in claim 1. In the first element of claim 1, the source or requesting device stores a retry bit associated with each stored request. In part C on the third page of the invention disclosure, Appellant states:

> The first retry transaction will have a special bit set in the header to indicate to the destination this is the first transaction that was retried.

Appellant discusses, in Part C on the third page of the Invention Disclosure, a "retry bit vector," each bit of which "corresponds to a source node that can send a transaction." The retry bit vector is clearly claimed in the second element of claim 1. A retry bit vector is a data structure, and data structures are generally stored in electronic memories. The third element of claim 1 regards storing of requests in a transaction queue until an ACK reply is received from the device to which the request is transmitted. Again, in part A of the Invention Disclosure, transaction queues are mentioned. In Part C of the Invention Disclosure, Appellant states:

> When the source gets the retry response, it starts to resend every transaction from the retried transaction onwards (since they are gong to be retried anyway).

If the source, or first electronic device, sends transactions in the order that they were initially sent, the source needs to store those transactions, such as in a request queue. In the third element of claim 1, retry bits associated with each stored request are used to mark requests for transmissions. In Part C of the Invention Disclosure, Appellant states:

> The first retry transaction will have a special bit set in the header to indicate to the destination that this is the first transaction that was retried.

In the fifth element of claim 1, the request-receiving device employs the retry vector to mark a second set of electronic devices that need to retransmit one or more rejected requests. Again, the retry vector is discussed in the first lines of section C of the Invention Disclosure:

> The proposed solution is to have a retry vector in the destination node that retries. Each bit in the vector corresponds to a source node that can send a transaction. Once set, the bit indicates that the source node has been retried for the ordered transactions in the particular flow-control class.

Thus, the currently claimed invention is fully and completely described in the Invention Disclosure submitted as Exhibit 1 with the initially filed Rule 131 Declaration. Appellant's representative can find no limitations in claim 1 that are not explicitly or implicitly covered by the Invention Disclosure. While it may surprise the Examiner that invention disclosures are as concise as the Invention Disclosure included with the Rule 131 Declaration, Appellant's representative assures the Examiner that, in fact, invention disclosures are commonly concisely presented, with the assumption that both in-house legal counsel and patent attorneys to which patent-application-drafting tasks are assigned are sufficiently familiar with the pertinent scientific and technical fields to understand the invention based on a concise disclosure. The Examiner is incorrect in stating that no invention disclosure was included in the Rule 131 Declaration, and is incorrect in stating that claim limitations are not supported by the invention disclosure.

ISSUE 2

2. Whether claims 1-20 are indefinite under 35 USC § 112, second paragraph.

The 35 U.S.C. §112, second paragraph rejections of claims 1-20 are detailed in the originally filed Appeal Brief, and Appellant's arguments and observations with respect to the 35 U.S.C. §112, second paragraph in the Appeal Brief remain reflective of Appellant's position. In this reply brief, Appellant responds to the Examiner's arguments under Issue 2 in the Examiner's Answer filed on March 24, 2006.

With regard to the 35 U.S.C. §112, second paragraph rejection of claim 1, Appellant's representative observes that, in the Summary of the Invention section of the current application, the context for claim 1 is clearly unambiguously stated:

> One embodiment of the present invention provides a method and system for straightforward and easily implemented flow control of ordered, pipelined transaction requests within a system of intercommunicating electronic devices. This embodiment of the present invention relies on information stored within a producing node, information stored within a consuming node, and information added to

> certain transaction requests as they are transmitted from the producing node to the consuming node. In the producing node, outstanding transaction requests are maintained within a source input queue, each transaction request associated with a retry bit. When a message is transmitted from the producing node to the consuming node, a special marker bit may be included to flag certain messages special to the consuming node. The consuming node maintains a retry vector having a retry bit corresponding to each producing node. When the producing node receives a NAK reply from the consuming node rejecting a transaction request, the producing node sets the retry bit for the transaction request in the source input queue, as well as the retry bits for other pending, subsequently received transaction requests directed to the consuming node. The producing node then proceeds to retransmit the transaction request and any additional pending, subsequently received transaction requests to the consuming node. When the producing node transmits the oldest transaction request pending for a particular consuming node, the producing node sets the special marker bit within the transaction request to flag the transaction request to the consuming node. When a consuming node receives a transaction request from the producing node, it first checks the retry vector to determine whether or not the retry vector bit corresponding to the producing node has been set. If so, then the consuming node responds with a NAK reply unless the special marker bit within the transaction request is set. If the special marker bit is set, and if the retransmitted transaction request can now be accommodated by the consuming node, the consuming node resets the bit within the retry vector corresponding node and replies with an ACK reply to the producing node. This technique guarantees that, once a consuming node rejects a transaction request within an ordered system of transaction requests, the transaction request will be retransmitted by the producing node in the proper order. (emphasis added)

Claim 1, as the Summary of the Invention, discusses an embodiment of the present invention with respect to a particular producing node and consuming node, within the context of a system of intercommunicating electronic devices. It is convenient to focus on one pair of intercommunicating entities, even though additional intercommunicating entities may reside within the system. Each transaction, for example, is generally conducted between a producing node and a consuming node, and the architecture of such systems is generally based on transactions. The phrase "a first set of electronic devices from which the second electronic device receives requests" explains that the retry vector includes a bit for each electronic device from which the second electronic device receives requests. A retry vector can only be explained in terms of a set of electronic devices that can send requests to the second electronic device. Otherwise, only a single bit would be needed, rather than a retry vector. Similarly, those electronic devices that need to retransmit one or more rejected

requests to the second electronic device are marked by retry-vector-bit-entry values. In general, not all of the first set of electronic devices, each represented by a bit within the retry vector, need to retransmit one or more rejected requests. Therefore, those electronic devices that do need to retransmit one or more rejected requests comprise a second set of electronic devices. Of course, in certain cases, and at specific points in time, the first set of electronic devices may be the same as the second set of electronic devices. The term "set" is used in the claim in the sense of a mathematical set. Claim 1 explicitly defines both the phrase "a first set of electronic devices" and the phrase "a second set of electronic devices." The Summary of the Invention clearly supports and provides context for claim 1. The first set of electronic devices includes the first electronic device mentioned in the preamble, since the first electronic device transmits requests to the second electronic device. The first electronic device mentioned in the preamble is included in the second set of electronic devices only when the first electronic device needs to retransmit one or more rejected requests to the second electronic device. Appellant's representative can find no ambiguity or lack of antecedent basis with respect to claim 1.

Appellant's representative has adequately explained Appellant's position with respect to claims 9 and 11 in the Appeal Brief. It is well known in communications and computing that electronic devices may be directly connected through a communications medium, or indirectly connected via two or more electronic communications media and intervening forwarding nodes. Claim 13 is self-explanatory. Claim 13 states that each bit of the retry vector corresponds to an electronic device that can send requests to the second electronic device. The first electronic device mentioned in the preamble can send requests to the second electronic device. Therefore, the first electronic device mentioned in the preamble is an electronic device that can send requests to the second electronic device. As made clear in the specification, the first electronic device and second electronic device specifically mentioned in the preamble reside within a system of intercommunicating electronic devices. As discussed above, and as clearly stated in the current application, a retry vector is needed within a receiving device in order to keep track of the retry status of each device within a system of intercommunicating electronic devices that can send requests to the electronic device.

With regard to the Examiner's comments directed to claim 15, Appellant's representative points out that a "system containing two intercommunicating electronic devices" is claimed. The fact that two electronic devices are intercommunicating implies that

they are directly or indirectly interconnected by one or more communications media. Intercommunicating electronic devices generally require communications media, communications protocols, signal lines, control registers, interrupt mechanisms, power supplies, and a host of other supporting physical and abstract logic structures and mechanisms. It appears that the Examiner would require a recitation of detailed aspects of such physical and logical structures to be detailed in a claim for a system of intercommunicating electronic devices. Such a requirement does not comport with current patent practice, the thousands of issued claims written by Appellant's representative, or the many thousands of issued patents that Appellant's representative has reviewed in the course of his practice. Moreover, there are myriad different ways of interconnecting to electronic devices, including specialized busses, serial links, packet-based communications media, and a host of other types of communications interconnections, including, in some cases, radio-frequency communications through free space via radio-frequency transceivers. Claim 15 is directed to a general system of intercommunicating electronic devices, rather than to specific communications media, protocols, configurations, and physical and logical implementations. Appellant's invention is applicable to a wide variety of different types of systems of intercommunicating electronic devices. Again, the fact that the electronic devices are intercommunicating implies that they are interconnected by one or more communications media, and such interconnections are well know and well understood in computer science and computing technologies. In the same fashion, a claim directed to a transmission in an automobile would generally not include recitation of engine components, including valves and cylinders, mufflers, tires, headlights, radiator, batteries, and other components, even though the transmission interconnects the engine with the power-consuming portions of the drive train. The tem "automobile" provides sufficient context for a specific claim directed to the transmission, or a component of the transmission, even though the transmission does not function apart from the other necessary components of the automobile.

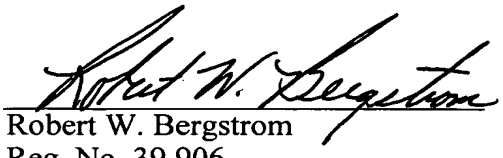
In an Office Action dated May 4, 2004, the Examiner rejected claims 1-20 under 35 U.S.C. § 112, second paragraph, as being indefinite. In a Response filed August 4, 2004, Appellant's representative endeavored to amend the claims to address certain of the Examiner's objections, and offered arguments that certain other of the Examiner's 35 U.S.C. § 112, second paragraph, rejections were unfounded. In the Final Office Action, dated July 21, 2005, the Examiner removed certain of the previous 35 U.S.C. § 112, second paragraph, rejections, and reiterated a majority of the rejections. Although Appellant's representative

believes that these rejections are unfounded, Appellant's representative endeavored to address them by amendment in a Response After Final, filed September 21, 2005. In an Advisory Action dated October 11, 2005, the Examiner refused to enter these amendments, stating that "[t]he amendments are the new issues, since they change the scope of the claims." Thus, it would seem that it is the Examiner's position that Appellant's only course of action, upon receiving a 35 U.S.C. § 112, second paragraph, rejection, is to agree with the Examiner, and correctly and fortuitously guess at an amendment that the Examiner would find to be acceptable, or to have the claims in question be finally rejected.

CONCLUSION

In Appellant's representative's opinion, the Examiner's statement that no invention disclosure was furnished with the originally filed Rule 131 Declaration is incorrect. The entire invention disclosure used by Appellant's representative in preparing the current application was provided as Exhibit 1 of the Rule 131 Declaration. Moreover, the invention disclosure completely described the essence of the currently claimed invention, with most claim limitations explicitly stated, and certain of the claim limitations implicit in the context of the invention provided by Appellant. With regard to the Examiner's 35 U.S.C. §112, second paragraph rejections, Appellant's representative believes that the current invention is clearly, distinctly, and correctly claimed by the current claims, which are fully supported by the current specification.

Respectfully submitted,
Debendra das Sharma
OLYMPIC PATENT WORKS PLLC

By 
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